CERTIFICATE OF MAILING

I hereby certify that this Transmittal is being deposited with the U.S. Postal Service, with sufficient postage, in an envelope addressed to the Board of Patent Appeals, Washington, D.C. 20231, on this 19 day of JUNE 2002.

Carol Giacomazzo

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION of Fallon et al.	:	Confirmation No. 2533
Serial No. 09/690,485	:	Art Unit 2841
Filed: October 17, 2000	:	Examiner: Jeremy Norris
Title: **TWO SIGNAL ONE POWER PLANE CIRCUIT BOARD**	:	

Atty. Docket No. END919960138US2 (IEN-10-5202-C1)

TRANSMITTAL OF APPEAL BRIEF

Board of Patent Appeals
Assistant Commissioner for Patents
Washington, D. C. 20231

Dear Sir:

1. Transmitted herewith in triplicate is the APPEAL BRIEF in this application with respect to the Notice of Appeal filed on April 23, 2002.

Note: "The applicant shall, within 2 months from the date of the notice of appeal under § 1.191 in an application, reissue application, or patent under reexamination, or within the time allowed for response to the action appealed from, if such time is later, file a brief in triplicate." 37 CVF 1.192(a) [emphasis added].

2. **STATUS OF APPLICATION**

This application is on behalf of

- ☒ other than a small entity
- ☐ small entity

Verified statement:

- ☐ attached
- ☐ already filed

3. **FEE FOR FILING APPEAL BRIEF**

Pursuant to 37 CFR 1.17(f) the fee for filing the Appeal Brief is:

☐	small entity	$ 160.00
☒	other than small entity	$ 320.00

Appeal Brief fee due: $320.00

4. **EXTENSION OF TERM**

Note: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of § 1.136 for patent application. 37 CFR 1.191(d). Also see Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 27 CFR 1.136 apply.

(complete (a) or (b) as applicable)

☐ (a) Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d)) for the total number of months checked below:

	Extension Months	Fee for other than small entity	Fee for small entity
☐	one month	$110.00	$55.00
☐	two months	$400.00	$200.00
☐	three months	$920.00	$460.00
☐	four months	$1,440.00	$720.00
		Fee:	

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

☐ An extension for _____ months has already been secured and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request $_____

or

☒ (b) Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. **TOTAL FEE DUE**

The total fee due is:

Appeal Brief fee	$320.00
Extension fee (if any)	$ 0.00

TOTAL FEE DUE: $320.00

6. **FEE PAYMENT**

☐ Attached is a check in the sum of $_____

☒ Charge **Account No. 09-0457** in the sum of **$320.00.** A duplicate of this transmittal is attached.

7. **FEE DEFICIENCY**

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency, if the maximum, six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

☒ If any additional extension and/or fee is required, this is a request therefor and to charge **Account No. 09-0457**.

AND/OR

☒ If any additional fee for claims is required, charge **Account No. 09-0457.**

Respectfully submitted,

Date: 6-19-02

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Title: **TWO SIGNAL ONE POWER PLANE CIRCUIT BOARD**	:	

Atty. Docket No. END919960138US2 (IEN-10-5202-C1)

Date of Final Office Action: January 30, 2002

APPEAL BRIEF

Board of Patent Appeals
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

REAL PARTY IN INTEREST

The real party in interest in the above entitled application is International Business Machines Corporation, having a principal place of business at Armonk, New York.

RELATED APPEALS AND INTERFERENCES

The undersigned attorney is not aware of any related appeals or interferences which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

STATUS OF THE CLAIMS

Claims 1-9 and 16-22 are pending in the present application. Claims 1-9, 16-18, 21 and 22 have been withdrawn from consideration. Claims 19 and 20 have been rejected and are the two claims on appeal. A copy of claims 19 and 20 is attached hereto as Appendix "A".

STATUS OF AMENDMENTS

An Amendment After Final Rejection was filed on March 12, 2002. This amendment did not propose any changes to the claims. This amendment did present a declaration of Ross W. Keesler under Rule 132, Mr. Keesler being one of the inventors herein. This amendment also presented additional arguments supporting the allowance of claims 19 and 20, in part based on the declaration of Mr. Keesler. The Examiner indicated that this amendment would be entered for the purpose of appeal, but continued the rejection of claims 19 and 20 on the same basis as in the final rejection.

SUMMARY OF INVENTION

The present invention discloses a method for forming a printed circuit card as well as the resulting circuit card. As a result of the Examiner's requirement for restriction and election, the present claims are directed to an embodiment of the circuit card. However, to understand the invention as claimed, a brief description of the method is included herewith.

Figures 2A through 2K show the steps in forming the circuit card which is shown in Figure 2K. A very brief description of these figures is included to enhance the understanding of the invention. In Figure 2A, a copper foil 20 is shown. An opening 22 is formed using either drilling or photolithographic and etching processes which are described on page 5, lines 12-24.

As shown in Figure 2B, a first layer of photoimageable dielectric material 24 is coated on one side of the copper foil and a second layer of photoimageable dielectric material 26 is coated on the opposite side of the copper foil 20, with the dielectric material filling the hole 22, as shown at 28. This is described on page 5, lines 25 through 29. In the preferred embodiment, the photoimageable material is an epoxy based material of the type described in U.S. Patent No. 5,026,624. The composition of the dielectric material is described on page 6, line 12, through page 7, line 2. Masks are applied over both the photoresist 24 and 26 to allow selective exposure of UV light to the photoresist materials 24 and 26. The sides are exposed through a mask, and then developed in propylene carbonate. This will provide openings 32 which extend to the surface of the copper foil. This will also provide openings 36 which are smaller in diameter than the openings 32 in the copper foil 20 to allow for a plated through hole. This is described on page 7, lines 2-12. A UV bump is then provided after the mask is stripped to fully cure the material 24 and 26. At this point and as shown in Figure 2D, both sides of the product are coated with photoresist 40 which is exposed and developed except where copper plating is to take place, as shown in Figure 2E. This is described on page 7, lines 27 and 28. Copper is then electrolessly plated, according to well known techniques, in the exposed areas through openings 42 and photoresist 40, which is shown in Figure 2F, to form circuit traces 44 on the dielectric material 24 and 26, blind vias 46 extending through the dielectric materials 24 and 26 and plated through holes 48. This is all shown in Figure 2F and described on page 8, lines 3-10. The photoresist 40 is then stripped, as shown in Figure 2G, and is described on page 8, lines 10-12. Figures 2H, 2I and 2J show additional steps which are not a part of the present invention and, finally, Figure 2K shows the metal foil 20 having a hole 22 therethrough and photoimageable material 24 and 26 on either side thereof with a hole 36 formed through the photoimageable material 28 in the hole,

with circuitry 44 and 46 on the photoimaged dielectric material 24 and 26, and a plated through hole 48 going from circuitry on one side to the circuitry on the other side.

ISSUES

Issue 1 – Is claim 19 anticipated under 35 U.S.C. 102(e) by Bhatt et al, U.S. Patent 5,822,856, hereinafter Bhatt et al?

Issue 2 – Is claim 20 unpatentable under 35 U.S.C. 103(a) over Bhatt et al?

GROUPING OF THE CLAIMS

Each of the claims presently in the application stands or falls on its own.

ARGUMENTS

Issue 1

With respect to the rejection of claim 19 under 35 U.S.C. 102(e), the Examiner states:

> "Bhatt et al (hereafter Bhatt) discloses, referring to figures 3-5, a printed circuit card comprising a metal layer (wiring layer 306) sandwiched between a pair of dielectric layers (310 & 312), said dielectric layers being formed of a photoimaged cured dielectric material (see the abstract), metalization on each of the first and second layers (wiring layers 506 & 304 respectively) forming circuitry on the first and second layers of the photoimageable material, and metal filled vias (hole 332, only one shown but a plurality referred to) in the first layer of photoimagable material (312) connected to the circuitry and the metal layer, and an opening (hole 328) in the metal layer and in the first and second layers of photoimageable material, the opening being metallized to connect at least a portion of the circuitry on the first layer with a portion of circuitry on the second layer without contacting the metal layer."

The Examiner in the rejection noted above states:

"said dielectric layers being formed of a photoimaged cured dielectric material (see the abstract)".

However, it is not believed this is an accurate representation of the layers 310 and 312. In the body of the specification if Bhatt et al, column 3, lines 66-67, it is stated:

> "...and three dielectric layers **308, 310, 312**. The dielectric layers may be ceramic or organic material.";

and in column 4, lines 39-45, the patent states:

> "In step **108** holes are drilled into the substrate through the peel apart structure. As shown in FIG **3**, hole **326** extends through the substrate and through both peel apart structures laminated to the surfaces of the substrate. Holes **328, 330, 332** are blind holes or cavities that preferably extend through the peel apart structure and into the substrate to buried wiring layers as shown."

While it is true that the abstract does refer to a photoresist layer, it is referred to in the following way:

> "A permanent dielectric photoresist layer is formed over the wiring layer and via holes are formed through the photoimageable dielectric over pads and conductors of the wiring layer."

This is described in further detail in the body of the Bhatt et al specification, column 6, lines 41-56 as follows:

> "In step **130** of FIG. **1***(d)*, a layer of first photoresist is formed over the continuous layer of metal. A liquid precursor may be spun on the surface and cured or more preferably a dry film photoresist 0.1 to 4 mils thick is used. In step **132** the photoresist is exposed to a pattern of electromagnetic radiation or a particle beam. The radiation may be produced in a pattern using a laser or a source of visible light, UV light, or X-ray which may be directed through a mask to form a pattern. The type of radiation or particle beam depends on equipment availability and the chemistry of the photoresist. In step **134** the photoresist is developed to form a first pattern of photoresist. The pattern covers portions of the metal layer which will form a wiring layer on the surface of the substrate. Other portions of the continuous metal layer are exposed and in step **136**, the exposed portions are etched away to form a first wiring layer (signal layer)."

As seen in the flow chart of Figures 1(a), 1(b), 1(c) and 1(d), forming the layer of photoresist and patterning the photoresist is *after* the step of plating the conductive material and copper foil to form a continuous copper layer on the surface. Thus, the reference by the Examiner to the abstract in no way teaches or suggests that the dielectric layers 310 and 312 must

be photoimageable as claimed. The Examiner points to alternative embodiments in Bhatt et al which indicates that there could be a substrate of dielectric polymer films, for example, polyimide. The Examiner states:

"polyimide is well known in the art to be a photoimageable material".

However, as pointed out in the declaration of Mr. Keesler, there are both photoimageable and non-photoimageable polyimides and there are different types of non-photoimageable polyimides. Thus, the statement that polyimides are photoimageable is not believed to be totally accurate. The statement, rather, should be that polyimides may be photoimageable. Moreover, Mr. Keesler states that, to his knowledge, photoimageable polyimides have never been used in any commercial product with IBM, and the Bhatt et al patent is assigned to IBM. Most importantly, however, is that there is no reference in the Bhatt et al patent to any type of photoimageable material other than the photoresist applied over the dielectric substrate. Bhatt et al only disclose a photoimageable material applied over the substrate in the form of a photoresist material which covers the circuitry on the dielectric layer. In any event, there is no suggestion or teaching anywhere within Bhatt et al that the underlying material, i.e. the dielectric substrate, is photoimageable.

In Shanklin Corporation v. Springfield Photo Mount Company, 521 F.2d 609; 187 U.S.P.Q. 129 (1st Cir. 1975), the court held:

"To anticipate under Section 102, a prior art reference must disclose all of the elements of the claimed invention or their equivalents functioning in essentially the same way. (615)

Similarly, the court in AMI Industries, Inc. v. EA Industries, Incorporated, 204 U.S.P.Q. 568 (DCNC 1979) also held that:

> "...it must be shown that the reference contains all of the elements of the claims apart from irrelevant or merely extraneous variations and the elements are arranged in the same way to achieve the same result which is asserted to be an inventive function."

Clearly, there is nothing in Bhatt et al which states that the underlying dielectric material must be photoimageable. Indeed, all of the examples cited are to non-photoimageable materials, which are either ceramic or organic, and the holes must be drilled since they cannot be photo-formed. Thus, it is submitted that there is no clear, unequivocal disclosure of a photoimageable dielectric substrate on which circuitry is formed. The best that can be said is that, in one of the alternative embodiments, the substrate might be photoimageable but there is no disclosure of such in Bhatt et al.

Thus, it is submitted that claim 19 is clearly not anticipated under 35 U.S.C. 102 by Bhatt et al.

Issue 2

Claim 20 has been rejected under 35 U.S.C. 103(a) as being unpatentable over Bhatt et al. In his final rejection, the Examiner states:

> "Bhatt discloses the claimed invention as described above with respect to claim 19 except for the limitation that Bhatt does not specifically state that the holes and vias in the dielectric material be photoformed. It would have been obvious, to one having ordinary skill in the art, at the time of invention, to photoform holes in the polyimide material as that is a well known conventional technique. Moreover, this limitation is a process limitation in a product claim and cannot serve to patentably define the product over the prior art of record. Furthermore, it is well settled that the presence of process limitations in product claims, which product does not otherwise distinguish over the prior art, cannot impart patentability to that product (*In re Johnson*, 157 USPQ 670, 1968)."

The Examiner admits that the holes and vias in the dielectric material of Bhatt et al are not shown to be specifically photoformed. The Examiner then states without any citation to authority that:

> "It would have been obvious to one having ordinary skill in the art, at the time of invention [was made] to photoform holes in the polyimide material as that is a well known conventional technique."

However, there is nothing within Bhatt et al that describes photoforming of holes. If indeed the Bhatt et al reference does teach the use of a photoformable material, it is only reasonable that Bhatt et al would have disclosed photoforming. However, Bhatt et al do not teach photoforming or suggest photoforming. The only teaching or suggestion within Bhatt et al is drilling of the holes. This further reinforces the notion that a photoimageable material is not contemplated by Bhatt et al. Moreover, even if one were to conclude that Bhatt et al do disclose a photoimageable material, nevertheless there is nothing within Bhatt et al, nor in any reference cited, that satisfactory vias could be formed by photoforming and filling with metal. Indeed, just because a material is photoformable does not necessarily indicate that it is capable of being photoformed in such a way as to provide vias which will provide interconnection between circuitry.

It is not enough that one may modify a reference, but rather it is required that a second reference suggest such modification of the first reference.

The CAFC stated In re Piasecki, 745 F.2d 1468, 223 USPQ 785, 788 (Fed. Cir. 1984) the following:

> "The Supreme Court in Graham v. John Deere Co., 383 U.S. 1 (1966), focused on the procedural and evidentiary processes in reaching a conclusion under Section 103. As adapted to ex parte procedure, Graham is interpreted as continuing to place the "burden of proof on the Patent Office which requires it to produce the factual basis for its rejection of an application under sections 102 and 103". Citing In re Warner, 379 F.2d 1011, 1020, 154 USPQ 173, 177 (CCPA 1967)."

The law is quite clear that in order for a claimed invention to be rejected on obviousness, the prior art must suggest the modifications sought to be patented; In re Gordon, 221 U.S.P.Q. 1125, 1127 (CAFC 1984); ACS Hospital System, Inc. v. Montefiore Hospital, 221 U.S.P.Q. 929,

933 (CAFC 1984). The foregoing principle of law has been followed in Aqua-Aerobic Systems, Inc. v. Richards of Rockford, Inc., 1 U.S.P.Q. 2d, 1945 (D.C. Illinois 1986). In the Aqua-Aerobic's case, the Court stated that the fact that a prior reference can be modified to show the claimed invention does not make the modification obvious unless a prior reference suggests the desirability of the modification.

In In Re Oetiker, 24 U.S.P.Q. 2nd 1443, 1445 (CAFC 1992) held:

> "There must be some reason, suggestion, or motivation found in the prior art whereby a person of ordinary skill in the field of the invention would make the combination. That knowledge can not come from the applicant's invention itself."

Most significantly, the CAFC in the recent case of In Re Dembiczak, 50 U.S.P.Q.2nd 1614 (CAFC 1999) held at 1617:

> "...(examiner can satisfy burden of obviousness in light of combination 'only by showing some objective teaching [leading to the combination]');"

Thus, it is clear that where an individual reference does not teach the entire invention, then the modification which the invention represents must be suggested and motivated by some other reference through some objective teaching and cannot come from the application itself, which is not the case here since there is but one reference cited. Hence, there clearly can be no suggestion of modifications in any way, let alone as suggested by the Examiner.

The statement by the Examiner that "Moreover, this limitation is a process limitation in a product claim and cannot serve to patentably define the product over the prior art of record" is not understood. The Examiner has not made a specific rejection as to this being an improper product by process claim, the only rejection being under 35 U.S.C. 103(a), which is related to obviousness. However, it is submitted that a process is not being claimed here but a specific hole which is photoformed. This a description of the hole per se and not a limitation to a process within the

claim. The hole is photoformed and a photoformed hole is different from holes formed by drilling. Moreover, the Examiner's statement "Furthermore, it is well settled that the presence of process limitations in product claims, which product does not otherwise distinguish over the prior art, cannot impart patentability to that product (*in re Johnson*, 157 USPQ 670, 1968)." is not understood and not believed to be accurate, since a photoformed hole is different from a hole which is drilled which is what is disclosed in Bhatt et al. Thus, these issues raised by the Examiner are not believed to be properly raised under 35 U.S.C. 103(a), nor are they believed to be accurate since this is not a product by process claim. The holes are defined as having been formed in a certain way but there is not process limitation in the claims.

SUMMARY

In view of the above, it is believed that both claims 19 and 20 are allowable over Bhatt et al, either as being anticipated by, or obvious over, Bhatt et al.

Respectfully submitted,

Date: 6-19-02

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Attachment

APPENDIX "A"

19. A printed circuit card comprising a metal layer sandwiched between a pair of dielectric layers, said dielectric layers each being formed of a photoimaged cured dielectric material,

metallization on each of said first and second layers forming circuitry on said first and second layers of said photoimageable material, and metal filled vias in at least said first layer of photoimageable material connected to said circuitry and to said metal layer and an opening in said metal layer and in said first and second layers of photoimageable material, said opening being metallized to connect at least a portion of the circuitry on said first layer with a portion of circuitry on said second layer without contacting said metal layer.

20. The invention as defined in claim 19 wherein said holes and vias in said dielectric material are photoformed.